ET420197753US

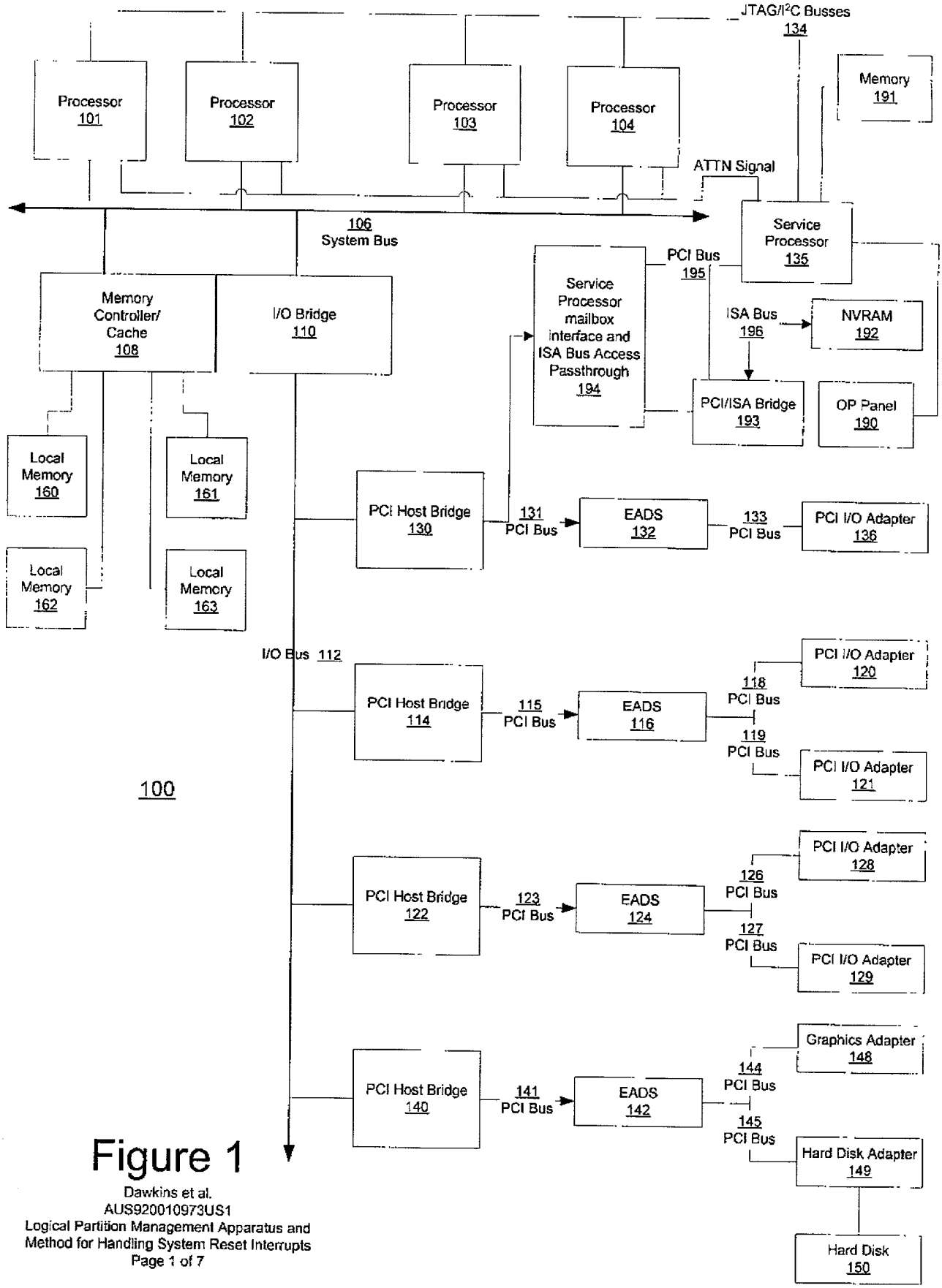

Figure 1

P04APP-748656AU

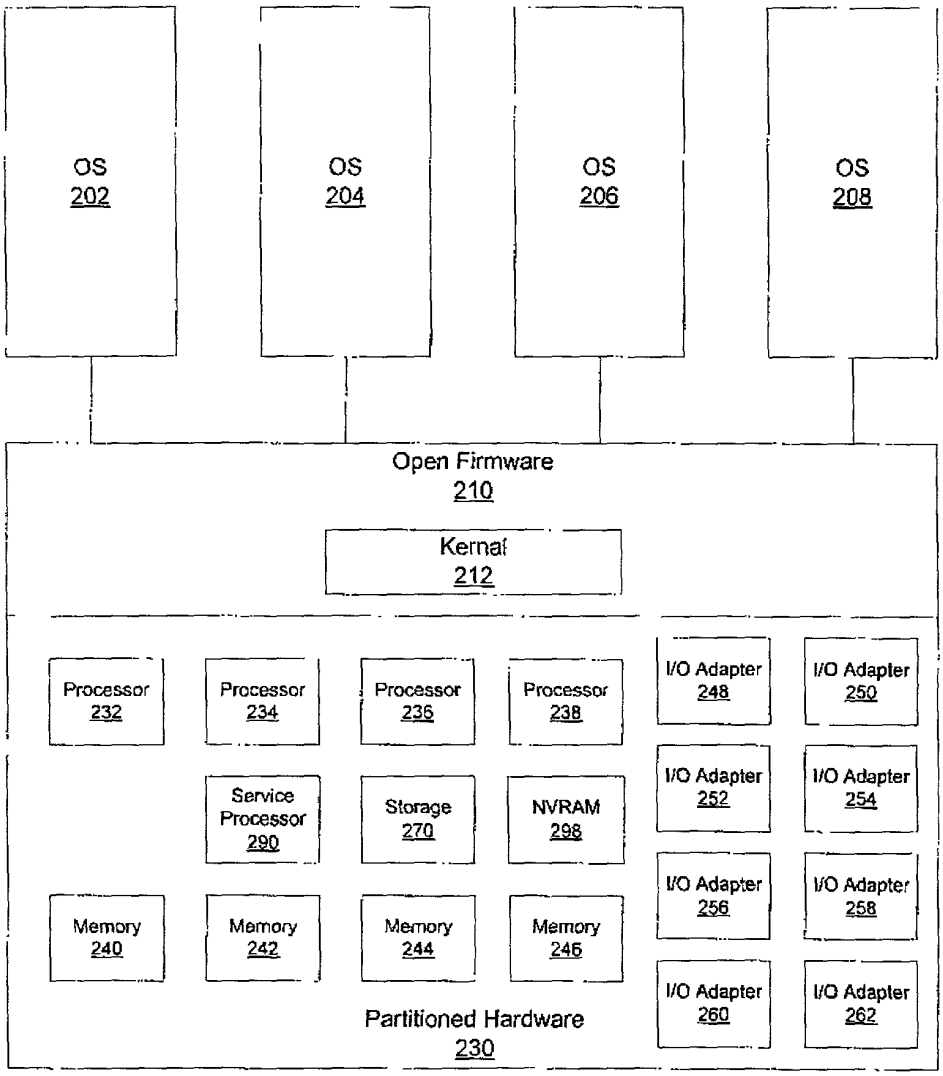

Figure 2

Docket: AUS920010973US1

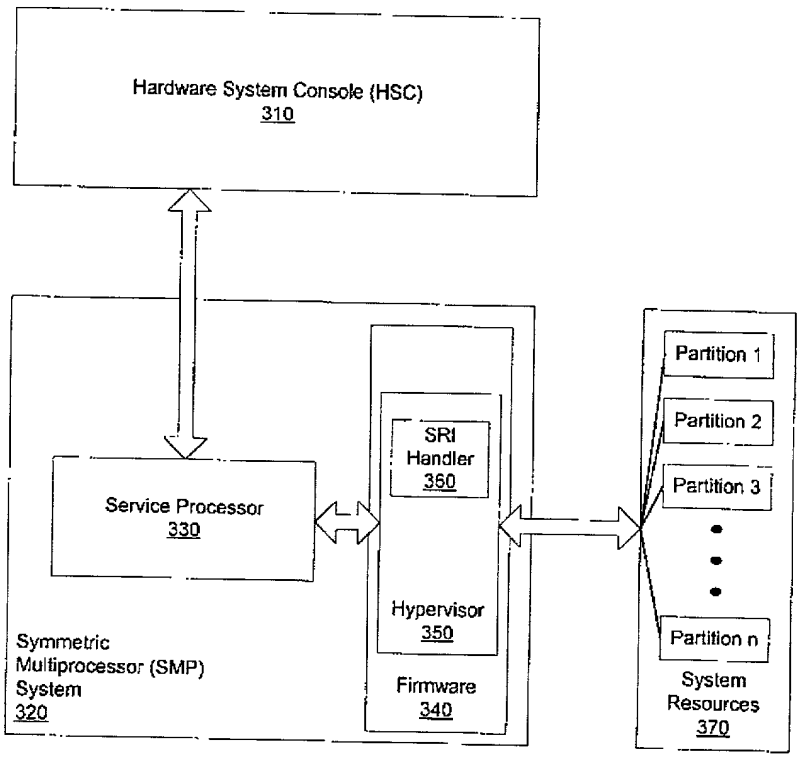

Figure 3

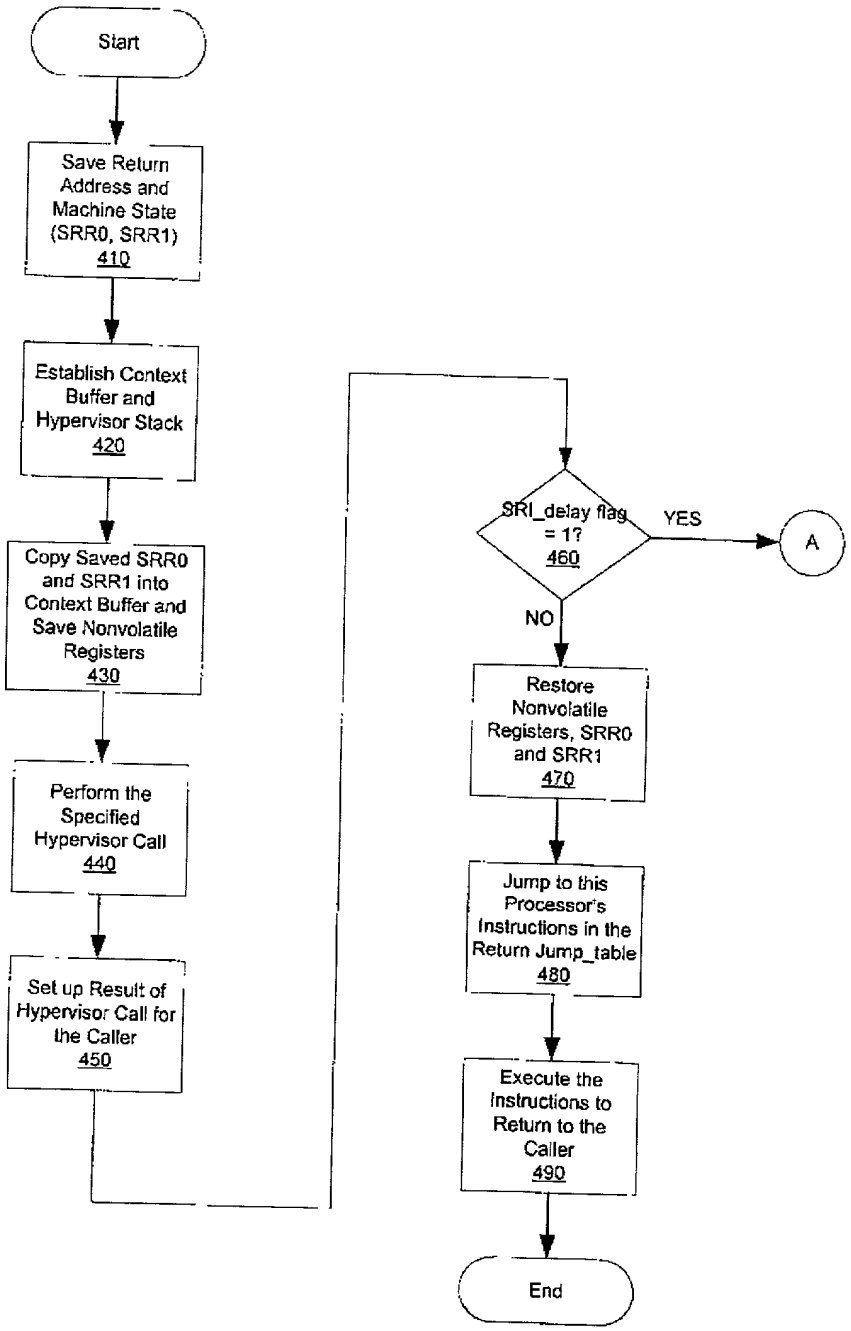
Start
Save Return Address and Machine State (SRR0, SRR1) 410
Establish Context Buffer and Hypervisor Stack 420
Copy Saved SRR0 and SRR1 into Context Buffer and Save Nonvolatile Registers 430
Perform the Specified Hypervisor Call 440
Set up Result of Hypervisor Call for the Caller 450
SRI_delay flag = 1? 460
YES
A
NO
Restore Nonvolatile Registers, SRR0 and SRR1 470
Jump to this Processor's Instructions in the Return Jump_table 480
Execute the Instructions to Return to the Caller 490
End

Figure 4

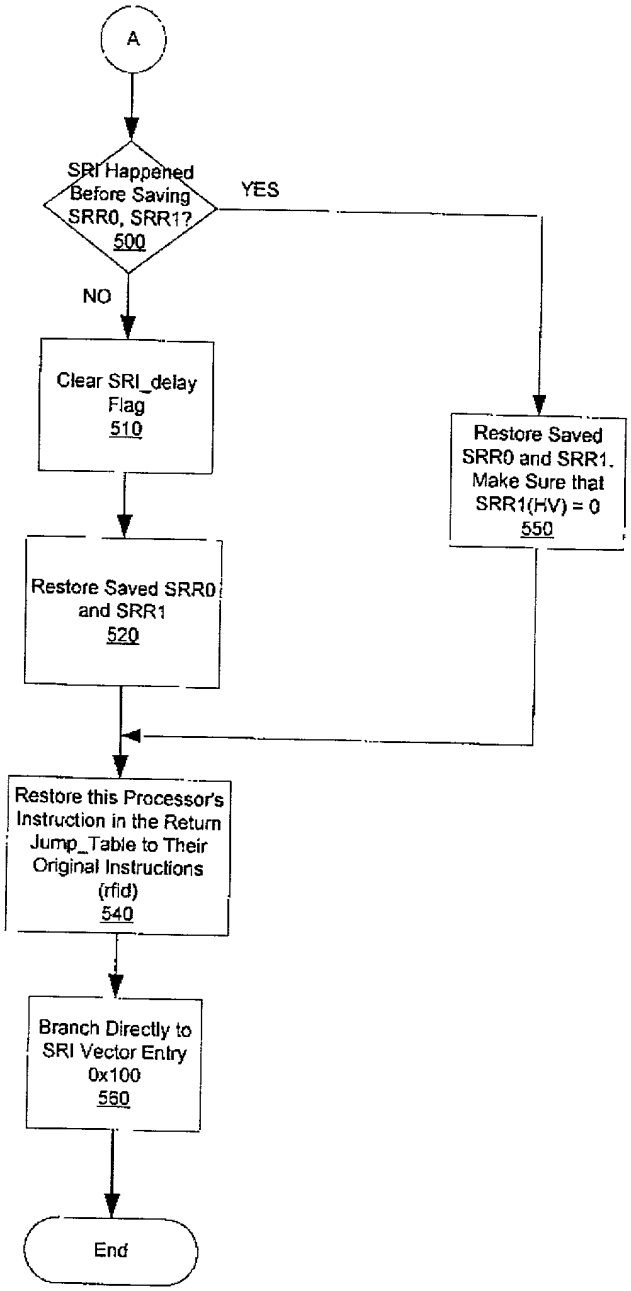
A
SRI Happened Before Saving SRR0, SRR1? 500
YES
NO
Clear SRI_delay Flag 510
Restore Saved SRR0 and SRR1. Make Sure that SRR1(HV) = 0 550
Restore Saved SRR0 and SRR1 520
Restore this Processor's Instruction in the Return Jump_Table to Their Original Instructions (rfid) 540
Branch Directly to SRI Vector Entry 0x100 560
End

Figure 5

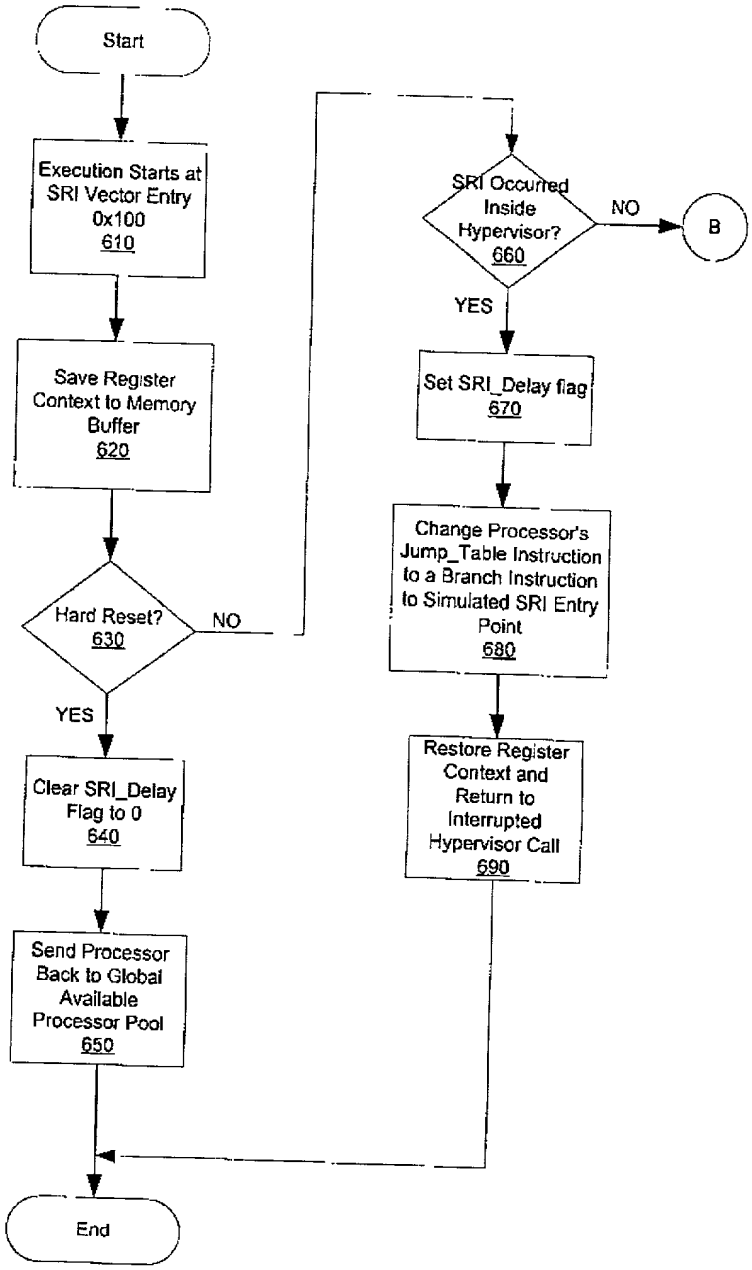
Start
Execution Starts at SRI Vector Entry 0x100
610
Save Register Context to Memory Buffer
620
Hard Reset?
630
NO
YES
Clear SRI_Delay Flag to 0
640
Send Processor Back to Global Available Processor Pool
650
SRI Occurred Inside Hypervisor?
660
NO
B
YES
Set SRI_Delay flag
670
Change Processor's Jump_Table Instruction to a Branch Instruction to Simulated SRI Entry Point
680
Restore Register Context and Return to Interrupted Hypervisor Call
690
End

Figure 6

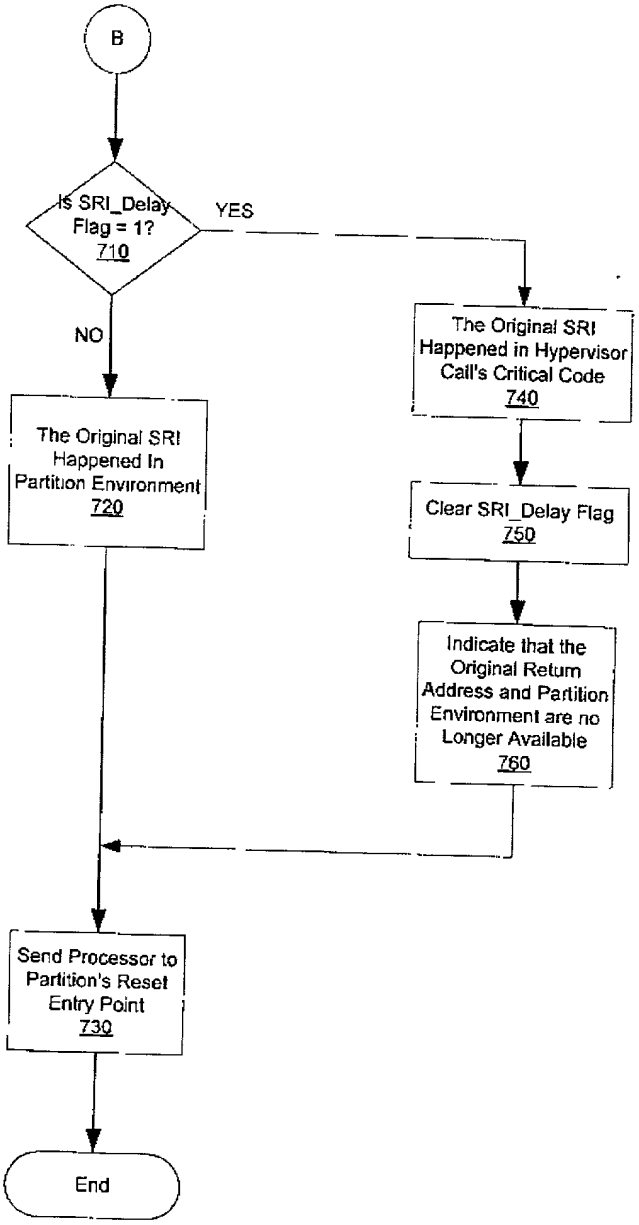
B
Is SRI_Delay Flag = 1? 710
YES
NO
The Original SRI Happened In Partition Environment 720
The Original SRI Happened in Hypervisor Call's Critical Code 740
Clear SRI_Delay Flag 750
Indicate that the Original Return Address and Partition Environment are no Longer Available 760
Send Processor to Partition's Reset Entry Point 730
End

Figure 7